REMARKS

This Preliminary Amendment is filed with a Request for Continued Examination and a two-month extension of time, filed on even date, and is in response to the Final Office Action mailed March 18th, 2004. All objections and rejections are respectfully traversed.

Claims 1-37 are now pending in the case.

Claims 35-37 have been added.

Claims 1, 11, 19, 20, 21, and 27 have been amended to better claim the invention.

Claim Rejections – 35 U.S.C. §102

At paragraphs 1-2 of the Office Action claims 1, 7, 11, and 19-21 were rejected under 35 U.S.C. §102(e) as being anticipated by Greim et al., U.S. Patent No. 6,163,829 (hereinafter Greim).

The present invention as set forth in representative claim 1 recites:

> 1. A system configured to acknowledge and service an interrupt issued to a processor of an intermediate node, the system comprising:
>
> an external device coupled to the processor by a high latency path, the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor;
>
> ***an interrupt multiplexing device accessible by the processor over a fast bus,*** the interrupt multiplexing device adapted to issue the interrupt

to the processor in response to each pulsed interrupt signal generated by the external device;

a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device; and

a status bit stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device,

wherein ***the processor acknowledges the issued interrupt without accessing the high latency path by accessing the interrupt multiplexing device over the fast bus.***

Greim discloses an interrupt handler that distributes interrupts among a plurality of processors. Devices issue interrupts on an external bus (VME bus, Fig 4, Item 12), to a VME interface (Fig 4, item 18), which intern conducts them to an interrupt controller (Fig 4, item 82). "The interrupt controller 82 is basically a steering device," that facilitates issuing the interrupts to multiple CPUs. (Col. 24, line 64 to col. 25, line 9). To acknowledge an interrupt, circuitry internal to the interrupt controller issues an interrupt acknowledge signal back to the VME interface over a bus (Col. 26, lines 56-57 and col. 29, lines 36-41).

Despite the of complexities of Greim, the reference essentially teaches a conventional method of acknowledging interrupts similar to the prior art method discussed in Applicant's specification. At page 15, lines 17-21, the Applicant comments "a conventional method for acknowledging and clearing the LSI signal involves the CPU issuing a read operation to the DMA controller to retrieve the contents of the DMA ISR 555." That is, a conventional interrupt acknowledge operation involves a read operation over a

high latency path to a DMA controller or similar device (ie. VME interface). Such a conventional operation introduces undesirable delays.

Applicant respectfully urges that Griem does not show Applicant's claimed invention relating to "***an interrupt multiplexing device accessible by the processor over a fast bus***", "***a low latency path coupling the external device to the interrupt multiplexing device***" and where "***the processor acknowledges the issued interrupt without accessing the high latency path by accessing the interrupt multiplexing device over the fast bus.***"

The Applicant's claimed novel invention reduces delays in interrupt handling by moving acknowledge operations closer to the processor. While Griem teaches acknowledging interrupts by first sending singles to the interrupt controller (internal multiplexing device) and then issuing interrupt acknowledge signals to the VME interface (external device), the Applicant teaches effectively acknowledging interrupts at an interrupt multiplexing device itself. Applicant's low latency path coupling the external device to the interrupt multiplexing device facilitates interrupt signals to be directly fed to the multiplexing device. Thereafter, the interrupts may be effectively acknowledged by an access to interrupt multiplexing device over the fast bus. As the Specification notes, "as a result, acknowledging and clearing of the interrupt signal no longer occurs over the high latency PCI bus 540, but rather takes place over the low latency fast device bus 532." Applicant's novel invention thereby more efficiently handles interrupts than conventional designs such as Griem.

Stated simply, Greim teaches returning acknowledgement signals from a processor to a VME interface. In sharp contrast, Applicant's claimed invention teaches acknowledging an interrupt at the interrupt multiplexing device (Greim's interrupt controller), thereby avoiding delays associated with accessing the DMA controller (Greim's VME interface).

Accordingly, the Applicant respectfully urges that Griem is legally insufficient to anticipate the presently claims under 35 U.S.C. § 102 because of the absence of Applicants' claimed novel "***an interrupt multiplexing device accessible by the processor over a fast bus", "a low latency path coupling the external device to the interrupt multiplexing device"*** and where ***"the processor acknowledges the issued interrupt without accessing the high latency path by accessing the interrupt multiplexing device over the fast bus."***

Claim Rejections – 35 U.S.C. §103

At paragraphs 3-5 of the Office Action claims 2-6 and 12-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim and Shek et al., U.S. Patent No. 6,185,652 (hereinafter Shek).

Applicant respectfully notes that claims 2-6 and 12-17 are dependent from independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 6 of the Office Action claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim, Shek, and Ecclesine, U.S. Patent No. 5,983,275 (hereinafter Ecclesine).

Applicant respectfully notes that claim 18 is dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claim is believed to be in condition for allowance.

At paragraph 7 of the Office Action claims 8-10 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim and design choice.

Applicant respectfully notes that claims 8-10 are dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 8 of the Office Action claims 1,7, and 19-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim and Swanstrom, U.S. Patent No. 5,754,884 (hereinafter Swanstrom).

Swanstrom describes a direct memory access (DMA) controller which services interrupt requests so that while a CPU is servicing one interrupt request the CPU cannot be interrupted by another interrupt request (Col. 10, lines 25-42). The interrupt requests and corresponding clear actions are transferred over a PCI bus to the DMA controller (Col. 11, lines 28-37, 52-53).

Applicant respectfully urges that Griem does not show Applicant's claimed invention relating to "***an interrupt multiplexing device accessible by the processor over a fast bus", "a low latency path coupling the external device to the interrupt multiplexing device"*** and where ***"the processor acknowledges the issued interrupt without accessing the high latency path by accessing the interrupt multiplexing device over the fast bus."***

Swanstrom teaches a conventional system where interrupt requests and acknowledgements are performed by accessing an external DMA controller. In sharp contrast, Applicant's teaches a low latency path to couple an external device to an interrupt multiplexing device, to facilitate interrupt signals to be directly fed to the multiplexing device. Thereafter, the interrupts may be effectively acknowledged by an access to interrupt multiplexing device over the fast bus leading to more efficient interrupt handling.

Accordingly, Applicant respectfully urges that Swanstrom and Greim, taken either signally or in combination, are legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 103(a) because of the absence of Applicant's "***an interrupt multiplexing device accessible by the processor over a fast bus", "a low latency path coupling the external device to the interrupt multiplexing device"*** and where ***"the processor acknowledges the issued interrupt without accessing the high latency path by accessing the interrupt multiplexing device over the fast bus."***

At paragraph 9 of the Office Action claims 2-6, and 12-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Shek.

Applicant respectfully notes that claims 2-6, and 12-17 are dependent from independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 10 of the Office Action claims 8-10 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and design choice.

Applicant respectfully notes that claims 8-10 are dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 11 of the Office Action claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim, Shek, and Ecclesine.

Applicant respectfully notes that claim 18 is dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claim is believed to be in condition for allowance.

At paragraph 12 of the Office Action claims 22-24, 27-29, and 32-34 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Okbay et al., U.S. Patent No. 6,606,677 (hereinafter Okbay).

The present invention as set forth in representative claim 22 recites:

> 22. A method for acknowledging and servicing an interrupt issued to a processor, the method comprising:

generating a pulsed interrupt signal at an external device;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device;

asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the pulsed interrupt signal;

issuing the interrupt to the processor over a second low latency path;

reading the status bit over the second low latency path by an interrupt handler internal to the processor; and

clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt.

Okbay discloses an interruptible bridge which interconnects two PCI busses. All interrupt requests and acknowledgements apparently pass between the two PCI busses and the interruptible bridge.

Applicant respectfully urges that Griem does not show Applicant's claimed invention relating to "***transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device***", ***"issuing the interrupt to the processor over a second low latency path"***, and ***"clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt."***

Okbay teaches a conventional system where interrupt requests and acknowledgements travel along PCI busses. In Sharp contrast Applicants invention novelly uses a low latency path to couple an external device to an interrupt multiplexing device, to facilitate interrupt signals to be directly fed to the multiplexing device. Thereafter, the interrupts

may be effectively acknowledged by an access to interrupt multiplexing device over the fast bus leading to more efficient interrupt handling.

Accordingly, Applicant respectfully urges that Swanstrom and Greim and Okbay, taken either signally or in combination, are legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 103(a) because of the absence of Applicant's "***transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device***", ***"issuing the interrupt to the processor over a second low latency path"***, and ***"clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt."***

At paragraph 13 of the Office Action claims 25 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Okbay, and Shek.

Applicant respectfully notes that claims 25 and 30 are dependent from a independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 14 of the Office Action claims 26 and 31 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Okbay, and Ecclesine.

Applicant respectfully notes that claims 26 and 31 are dependent from a independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

All independent claims are now believed to be in condition for allowance.

All dependant claims are believed to be dependant from allowable independent claims.

The Applicant therefore respectfully requests favorable action.

The Applicant earnestly solicits the Examiner to contact the undersigned by telephone at 617-951-3078 to advance the prosecution of the application in any respect.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

James A. Blanchette
Reg. No. 51,477
CESARI AND MCKENNA, LLP
88 Black Falcon Avenue
Boston, MA 02210-2414
(617) 951-2500